OSDTM: an Offline-Structural Distributed Test Mechanism for Data Links in NoC

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Abstract— **The Micro Packet Switched based Network on Chip (NoC) is emerged to address traditional non-scalable buses-based Systems on Chip (SoC) challenges such as out of order transactions, flow control and higher latencies. The NoC is disposable to a different of defects in its life which cause of such drawbacks as data missing, efficiency reduction, and eventually, entire system overwhelm. This paper is amid to propose a new Offline-Structural Distributed Test Mechanism (OSDTM) to discovering and emplacing shorts on the data links in NoC. The projected test approach encompasses three main component namely Test Pattern Producer (TPP), Test Response Compiler (TRC) that are implanted in the Network Adapter (N) as well as a Flit Comparator Block (FCB) located in the Routers(R). The FCB concern is to detect dissimilar Flits through comparison the entrance Flits. The OSDTM leads to 100% Test Coverage (TC), 82.3% Discovering Capability (DC), and 100% fault emplacement (FE) of faulty links in NoC. The experimental results illustrate that the FCB hardware cost is very insignificant in related to the hardware of Vici router.**

Keywords-component; Network on Chip; Biult in self test; links test mechanism; fault discovering and emplacement;

I. INTRODUCTION

The packet-switched based Network-on-Chip (NoC) is emerged to address traditional non-scalable buses-based Systems on Chip (SoC) challenges such as out-of order transactions, high power consumption, higher latencies, and end-to-end flow control [1-5]. The NoC includes a set of Routers (R), Links (L), Intellectual Property (IP) cores, and Network Adapters (NA) [6, 7]. The Routers are connected to each other with point-to-

point Links due to one or more, homogeneous or heterogeneous processing elements (PE) more which is known IP cores, is clustered to a On one hand, the growing number of routers and channels and the lessening chip size and on the other hand to handle the requirements of bandwidth have made NoC prepared to such permanent faults on channels as short faults, open faults, and stuck at fault [11]. Each of these faults have a unique effect upon the NoC. The short fault on a single channel clues to overloading, dropping, packet replication, misrouting, delay which therefore

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damagingly effect on the network performance. Therefore, it seems vital to discover and place short faults on channels to prevent the reduction of NoC efficiency.

A considerable number of studies have been carried out in regarding to channel test, which will be illuminated in the subsequent section. Built-in Self-Test (BIST) is one of more commonly mechanisms. This approach is thought to be cost-effective and widespread for such various proofs as test efficiency with the unnecessity of external test equipment, circuit speed, and online and offline testing [12]. In this mechanism, Test Pattern Producer (TPP) on the one hand of the unidirectional channel creates test patterns and puts to it; and on the other hand, Test Response Compiler (TRC) capture and compiles the test results. The two blocks are needed to be implanted both in router (i) and router (j) until the bidirectional channels between the routers i.e. (R_i, R_j) to be tested, consequently [13]. In addition, both units must be placed in NA for testing the bidirectional channel between the router and NA i.e. (NA_i, R_i) [14]. In NoC, every router and NA needs a twosome of TPP and TRC. However, the hardware plenty rises significantly with an increase in the network size. The methods suggested for channels testing have not managed to prevent the rising or falling of such parameters as, test coverage, test time, fault discovering, and fault location capabilities. Each research, however, is projected to offer a balance between these parameters. Furthermore, the methods suggested for testing of NoC have not clearly negotiated how to tolerate the fault by knowing fault information.

This paper proposes an offline-structural BIST-based approach for channels in NoC with fault emplacement and best test envelopment, and minimum hardware penalty which is capable of directing the short-faults in channels. The OSDTM is able to coverage 100% of data links and to emplace 82.3% faulty channels by forming a *to-Neighbor Vectors (tNV)* in NOC as well as implanting an ordinary collation block in the router. The contributions of the OSDTM are:

- The TPP and TRC units have been removed from the router; this impressively decreases the hardware penalty in the previous mechanisms.

- In OSDTM, by concurrent execution of test process in all links, the Test Time (TT) and Test Period (TP) is reduced.

The current paper is prearranged as follows: we summarize recently related works in Section 2. Short faults model is explicated in section 3. The OSDTM is provided in section 5. Fault coverage, in section 6, hardware redundancy in section 7, and test time in section 8 are clarified. Finally, simulation results, conclusions and future works are discussed in section 9 and section 10 respectively.

II.   RELATED WORKS

The test is a process in micro Network on chip to detect producing defects and living faults that is typically partitioned to two sub process: 1. IP cores testing 2. Communication infrastructure testing. Generally, in the IP core testing, NoC has been reused as TAM [3, 15-20] to decrease the test penalties. The communication testing is divided to two sub process namely; router test and channels test. The important works e.g. [21-28] is carried out in routers testing. In communication testing, some concepts such as stuck-at, short, and open and delay fault [29-32] as well as transient faults (crosstalk) [33] have been brought from System-on-Board(SoB) literature. In [34] Raik et al. offer an outside test mechanism that is testing the routers and links to discover short, open, and delay faults functionally. A BIST based and at-speed testing for the links between the routers is proposed by Grecu et al. in [13]. The provided approach targets crosstalk faults and short faults by assuming the MAF fault model [33]. The test vectors are embedded in payload flits and are conducted to links being tested. Therefore, by parallelization of test process, they plan to decrease the test time. In [35], a functional and scalable BIST based mechanism that is testing inter router links to discover physical faults is presented. One of the most exhaustive works to discover shorts in data and handshake links in the communications test is provided by Cota et al. in [14]. The authors implanted the TPP and TRC in the Network Interface and discovered the short faults via producing test flits, conducting to neighbors, and compiling the outcomes. The proposed approach do not determine the faults location, by consider the hardware penalties are decreased. In [36] Herve et al. plan to discover 93% of the short faults in the links resulting to optimize their later fault discovering mechanism. Their offered approach, hence, resolved problems of fault emplacement. Likewise, in [37] the authors use this approach for a mesh topology. The BIST based approach contains the discovering and diagnosing of short faults in links by enabling another path for the damage links. In [38], Herve et al. combine the functional test [37] with the routers test. In [39], the authors present a self-diagnosis and BIST based approach for testing of stuck at faults. Kakoee et al. in [40], is suggested an online test approach to links that the routers by cooperation each other are able to discover stuck at and short defects in intra-routers links. In [41] the authors declare an online test discovering and debugging approach by collecting error syndrome and counting flits for control and data links. In [42], a discovering and debugging approach for short, stuck at, and delay faults in the Network Interface and links. Recently, an on-line approach for finding the short faults in the links is provided by Bhowmik et al. in [43-45]. They execute simulation in some period and evaluate the parameters such as power consumption, throughput, and delay. We reviewed a lot of works but there are a few works are addressed the fault discovering in NA and Router links. Some mentioned works, increasingly lifts the system's hardware redundancy and also various setting need for the implementation. Furthermore, there are some studies which likely have not directed how the test information are used for faults emplacement.

III.   SHORT FAULT MODEL

In single channel, when *w* wires is adjoined to each other a short fault is formed which result to wires junction in both direction links of Router-Router (R, R) and Router-NA (R, NA). Short faults are divided into two type: OR-short, and AND-short. Locally, these faults are categorized in two types of intra-channels

shorts and inter-channels shorts [44]. The current work focus on second fault type. In Fig.1, the shorts of router-router link (R_a, R_b) is depicted.
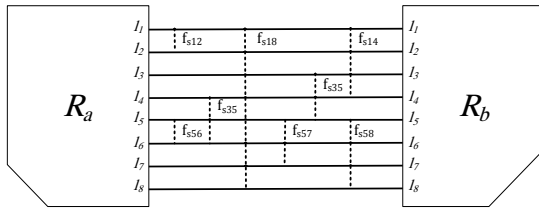

Fig.1. Router-Router (R_a, R_b) Shorts

As shown in Figure 1, fs_{ij} is employed to explain a short between the two l_i and l_j wires. Via Eq. 1, everyone can to evaluate the number of shorts in the link with the n wires [45]:

$$Ns = \sum_{k=2}^{n} \frac{n!}{k!\,(n-k)!} \qquad (1)$$

So, a one-way link with 10 wires equals with 1013. Generally, shorts in a NoC with Ch links is calculated by Eq. 2.

$$Nnoc = Ns \times Ch \qquad (2)$$

IV. OFFLINE-STRUCTURAL DISTRIBUTED TEST MECHANISM (OSDTM)

As mentioned, this paper is aimed to find and emplacing the shorts of a link. The OSDTM is capable to range from a two by two to N by N Mesh topology with every length. The benefits such as concurrent data conveyance, regularity, and reined electrical factors the Mesh topology is selected [46]. Furthermore, the industries and research communities are employed Mesh topology [3, 47]. The OSDTM can be classified into five concepts: 1) Test Packet, 2) to-Neighbor Vectors, 3) fault location, 4) Flit Comparator Block, and 5) test approach.

A. Strucrure of Test Packet

the most common test vector for discovering the shorts in link with w wire is Walking-One (W-ONE) sequence [48] which is generated by TPP. The Network Adapter wraps head, W-ONE, and tail in the format of a packet. This packets is broken to Flits and is applied to links that needed to be test. Typically, the head information including beginning packet, aim address, and available request to the link, the flow control, and the packet kind. Also, Final packet and link permission are the two main tail information. The size of packet varies based on link width w. in this paper, it is considered $w=10$. Figure 2 illustrates a typical test packet.

Fig.2. Test packet structure

Header Flit	Walking-one	trailer Flit

B. to-Neighbor Vectors(tNV)

The term of *to-Neighbor Vectors* is a kind of Flit broadcasting. For performing the presented mechanism (OSDTM) it is vital to establish this type of traffic. The tNV has the following characteristics:

- TPPs are responsible to generate test Flits (containing test vectors).

- The Network Adapter broadcasts the Flits to the whole of its neighbors.

- Every Flit crosses three links to be received by neighbor.

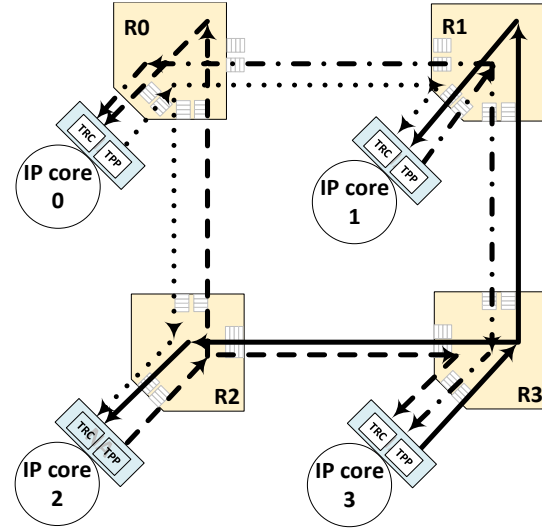Fig.3 depicted tNV traffic on a 2×2 Mesh NoC.

Fig.3. the tNV traffic

Totally, current paper is divided the routers type from aspect port number in three types: 1) 3-doorway, 2) 4-doorway and 3) 5-doorway. All of IP cores are generating Flits according to the tNV, so the whole of routers doorways are either sending or receiving the Flits. Consider that equivalent tNV traffic is established in network; every router will cashing the same flits from doorways. Therefore, the 3-doorway router, the 4-doorway router, and the 5-doorway router will receive 3, 4, and 5 equal Flits, in ordinal. If a router gain an unlike Flit from one of its doorways, this consider: "A defect has happened in the route that the Flit has crossed.

C. Fault Location

The paths a Flit crosses to attain R2 (i.e. i0, i1, and i2) are clarified by the lines in Fig.4. The i0 is a single link of (N_2, R_2), but also, i1 comprises two links of (N_0, R_0) and (R_0, R_2), and i2 includes two links of (N_3, R_3) and (R_3, R_2).zFig.4. A typical router input routes in the tNV

When the router receives 3 equal flits from its 3 doorway then suppose no fault is occurred. But, if a flit is different from the rest then a defect is happened in the touts crossed.

For example, if the Flit logging from i1 path be different other Flits, then a defect is occurred in one or both links (N_0, R_0) and (R_0, R_2). In Table 2, we survey all of possible situations and positions. For the 4-doorway and 5-doorway routers also one can develop a table same as Table 2.

Table 2. Fault emplacement in 3-Doorway router 2×2 Mesh NoC

Doorways			Positions							
			R_0		R_1		R_2		R_3	
i2	i1	i0	Faulty	faultless	Faulty	faultless	Faulty	faultless	Faulty	faultless
0	1	1	(N_1,R_1) (R_1,R_0)	(N_2,R_2) (R_2,R_0) (N_0,R_0)	(N_0,R_0) (R_0,R_1)	(N_3,R_3) (R_3,R_1) (N_1,R_1)	(N_3,R_3) (R_3,R_2)	(N_0,R_0) (R_0,R_2) (N_2,R_2)	(N_2,R_2) (R_2,R_3)	(N_1,R_1) (R_1,R_3) (N_3,R_3)
1	0	1	(N_2,R_2) (R_2,R_0)	(N_1,R_1) (R_1,R_0) (N_0,R_0)	(N_3,R_3) (R_3,R_1)	(N_0,R_0) (R_0,R_1) (N_1,R_1)	(N_0,R_0) (R_0,R_2)	(R_3,R_2) (N_3,R_3) (N_2,R_2)	(N_1,R_1) (R_1,R_3)	(N_2,R_2) (R_2,R_3) (N_3,R_3)
1	1	0	(N_0,R_0)	(N_1,R_1) (R_1,R_0) (N_2,R_2) (R_2,R_0)	(N_1,R_1)	(N_0,R_0) (R_0,R_1) (N_3,R_3) (R_3,R_1)	(N_2,R_2)	$(N_0,R0)$ (R_0,R_2) (N_3,R) (R_3,R_2)	(N_3,R_3)	(N_1,R_1) (R_1,R_3) (N_2,R_2) (R_2,R_3)
1	1	1	-	(N_1,R_1) (R_1,R_0) (N_2,R_2) (R_2,R_0) (N_0,R_0)	-	(N_0,R_0) (R_0,R_1) (N_3,R_3) (R_3,R_1) (N_1,R_1)	-	(N_0,R_0) (R_0,R_2) (N_3,R_3) (R_3,R_2) (N_2,R_2)	-	(N_1,R_1) (R_1,R_3) (N_2,R_2) (R_2,R_3) (N_3,R_3)
1	0	0	No Detectable								
0	0	0	No Detectable								
0	0	1	No Detectable								
0	1	0	No Detectable								

1: faultless Flit 0: faulty Flit

It is worth to note the supposal that all network links simultaneously be defect does not look genuine [14]. According the table 2, when the router get two or three equal Flit then can be discovered the faults. Furthermore, the router is capable to locate one faulty links. Suppose the number of router inputs as d, then $d-2$ defect can be emplaced. So, this quantity is supposed *as discovering threshold (DT)*. According to the DT of each router, a few situations (See Table 2) is produced in the FCB. In a few situations the defects can be emplaced, however, in a few cannot be. Suppose $S_{discoverable}$ is the number of discoverable situations and $S_{undetecable}$ is undiscoverable ones, so the discovering capability i.e. DC, can be calculated by Eq.3:

$$DC = \frac{S_{discoverable}}{S_{dscoverable} + S_{undiscoverable}} \qquad (3)$$

The discovering capability quantity for each router is computed in Table 3.

Table 3. The discovering capabilities of all router types

Router	discovering Threshold (p-2)	Situations		DC
		Discoverable	Undiscoverable	
3-doorway	1	4	4	50%
4-doorway	2	11	5	68.75
5-doorway	3	26	6	81.25

D. Flit Comparator Block (FCB)

So that to contrast the reached flits a flit comparator block is needed. FCB is a combinational circuit which is developed from XOR gates. The input and output of the FCB are in both parallel and serial. The FCB parallel inputs is mapped to input doorways of routers and also the FCB parallel outputs to output doorways. If a fault occurs in (N_i, R_i) link, the FCB to prevent the fault propagation to other paths, release the faultless link's Flit-determined by analogy-to output doorways except local doorway. The serial input and output of FCB are supposed to scan based tests. We do not focus on the test of FCB. Fig.5 depicts the FCB conjunctions with router doorways.
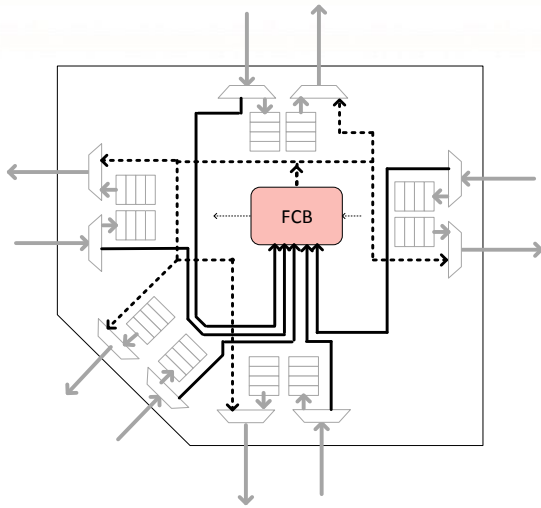
Fig.5. Flit Comparator Block

It may be the case that the defects with same effects can occur on the links and FCB wrongly suppose link as faultless. We answer this as following; As mentioned the number of shorts in a simple link with w=10 wire is $N_s = 1013$. As result, the feasibility for the same impact of two fault in one link is 1/1013.

It suppose the two Flits logged from i_0 and i_1 paths are the same; so, the probability of a same fault happens on i_0 and i_1 inputs $P(i0_{faulty} = i1_{faulty})$ equals:

$$P(i0_{faulty} = i1_{faulty}) = P(i0_{ch} \cap i1_{ch1} \cap i1_{ch2})$$
$$= P(i0_{ch}) \times P(i1_{ch1}) \times P(i1_{ch2})$$
$$= \frac{1}{1013} \times \frac{1}{1013} \times \frac{1}{1013}$$
$$= 9.6e - 10$$

Similarly, for evaluation of the probability of a same fault on i_1 and i_2; $P(i1_{faulty} = i2_{faulty})$ we have:

$$P(i1_{faulty} = i2_{faulty})$$
$$= P(i1_{ch1} \cap i1_{ch2} \cap i2_{ch1} \cap i2_{ch2})$$
$$= P(i1_{ch1}) \times P(i1_{ch2}) \times P(i2_{ch1}) \times P(i2_{ch2})$$
$$= \frac{1}{1013} \times \frac{1}{1013} \times \frac{1}{1013} \times \frac{1}{1013}$$
$$= 9.5e - 13$$

Needless to say, of 1013 faults, there exist defects that maybe have the same effects on the link. To description that, even understanding this matter, when the FCB demonstrates the equality of two Flit; it means two faultless path rather than two path with the same faults. We can popularized to 4-doorway and 5-doorway routers as well.

E. Test Approach

Two feasible approach can be used to run OSDTM: 1) zonal test and 2) universal test. In the zonal approach, the NoC is portioned into some zone in which the defection scanning is performed. The whole NoC can be distributed into 2×2 Mesh NoC via several setting; and every Mesh network can be tested in various test steps. Some works are applied this approach [14, 36-38]. In the universal test, the total of network is verified by a simple setting. Total links, in this mechanism, are concurrently glutted with test vectors and then the

outcomes are captured. According to the tradeoff test period and the NoC efficiency, one of these methods is chosen. In the current article, the universal verification to execute OSDTM is employed. One period (two execution steps) are needed filling out the verification:

Step 1: In this phase, TPP_0, TPP_1, …, TPP_n are producing test Flits with same vectors of $W\text{-}ONE_0$, $W\text{-}ONE_1$, ..., $W\text{-}ONE_n$ and propagate them in NoC. On the other side, TRC_0, TRC_1, ..., TRC_n obtain the result and compile them. The Flit including $W\text{-}ONE_0$, according to tNV, crosses through the three links of (R_1, N_1), (R_0, R_1), and (N_0, R_0) to relocate from TPP_0 to TRC_1. Each FCB, besides, gets test Flits and then verifies the table states. In this level, the two situations of table (i.e. "111" and "110") are verified. The "111" situation means total path's links are faultless. If the FCB determines the "110", then a defect has happened in the (N_i, R_j) link.

It is worth to note the (R_i, N_i) link has not been verified (see Table 3) because this is one on the duties of TRC placed in the Network adapter. After the FCB could discovering faultless Flit conducts it to the (R_i, N_i) link and then the TRC determines on it as either being faulty or faultless. By this scenario, we can judge on the (R_i, NA_i) and (NA_i, R_i) links in total NoC.

Step 2: This step is similar to first step. In this step, the situations "011" and "101" are verified because the verification of (NA_i, R_i) link is carried out in step 1. The upper two situations, therefore, characterize the defect on the (R_i, R_j) link. Totally, in step 2, we can judge on links between routers as either faultless or faulty. Let's to anamnesis, when FCB discovers a defect in step 1, on the (N_i, R_i) link, then propagates the faultless Flit to the output doorways (except local doorway). Totally, the defects on links among the Router-Network Adapter and Router-Router are discovered and emplaced in steps 1 and step 2.

V. DISCOVERING CAPABILITY

In 3-doorway routers, generally, OSDTM in step 1 and step 2 verifies two links in test period. The OSDTM verifies in 4-doorway routers in step 1 two links and in step 2 three links and in 5-doorway routers in step 1, two links and in step 2 four links. Discovering capability is the quantity to calculate the number of tested links in one test round. Totally, the discovering capability in OSDTM, equals 100% in the end of test round. The discovering capability in two steps for various NoC dimensions is illustrated in Fig.6.
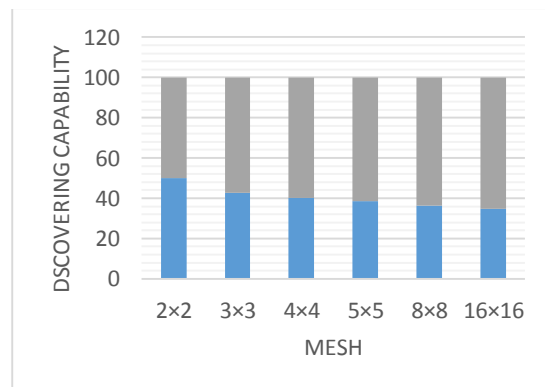

Fig.6. Discovering capability (%) in step 1 and step 2.

The DC for various NoC sizes is calculated in Table 4.

Table 4. Discovering Capability (DC) in OSDTM

Size	#Bidirectional links	#Routers			#Core	Emplaced faulty links	DC
		3-d	4-d	5-d			
2×2	16	4	0	0	4	10	62.5%
3×3	42	4	4	1	9	30	71.4%
4×4	80	4	8	4	16	60	75%
5×5	130	4	12	9	25	100	76.9%
8*8	352	4	24	36	64	282	80.1%
16*16	1472	4	56	196	256	1211	82.3%

VI. HARDWARE CONSIDERATIONS

For implementing OSDTM on a NoC-based system, basically, three hardware blocks are redundant: 1) FCB, 2) TPP, and 3) TRC. The FCB is implemented on ISE Xilinx [49] with Spartan 3E platform [50] and hardware penalties is calculated. The simulation outcomes are specified for all three routers in Table 5. Furthermore, the hardware redundancy in approach proposed has been compared with the Vici router hardware (20,413 gates) [51].

Table 5. The OSDTM hardware penalties

Router	FCB		Vici [51]
	LUT	BELS	
3-port	69	76	0.37%
4-port	144	165	0.8%
5-port	262	313	1.5%

In the OSDTM, the TPP and TRC, have been removed from the routers and instead a FCB has been putted. However, each Network Adapter contains a couple of TPP and TRC. Based on implementation of TRC and TPP in [36], we consider TRC has 341 gates and TPP has 401 gates. Generally, Table 6 is demonstrated the hardware overhead in OSDTM for several NoC sizes.

Table 6. The NoC hardware redundancy

Mesh	All channels	Our proposed method					Network Hardware Redundancy (Gates)
		TPP	TRC	FCB			
				P3	P4	P5	
2×2	16	4	4	4	0	0	3196
3×3	42	9	9	4	4	1	7947
4×4	80	16	16	4	8	4	14748
5×5	130	25	25	4	12	9	23651
8×8	352	64	64	4	24	36	63000
16×16	1472	256	256	4	56	196	260842

VII. TEST TIMING

In this paper, we are supposed the tester is a distributed test program that is executed on all IP cores. The test program controls the test process. The test time is identified as the time among the first Flit is generated in TPP and the last Flit compiled in TRC. According OSDTM, it is necessary the Flits containing W-ONE vectors to pass all links and routers. In each step, consequently, one test packet is generated and released in the network. The packets are generated simultaneously to enhance parallelization and to reduce the test time. Fig.7, in detail, depicts the signals and exchanged data in a 2×2 Mesh NoC.
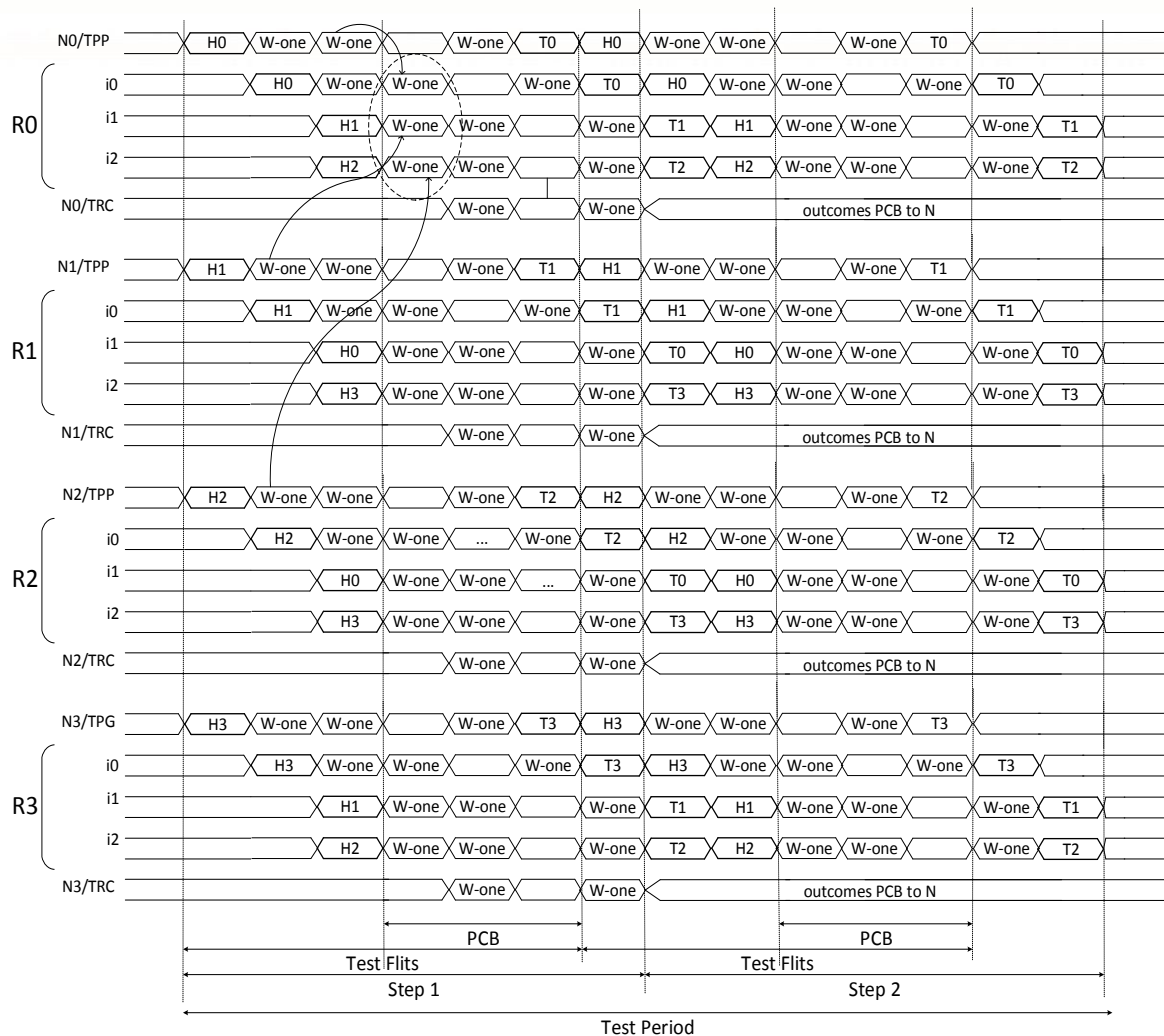
Fig.7. OSDTM timing

Simultaneously, the TPPs in NoC are producing the test vectors and the TRCs compiles the results. Let's see the TRC signal, in step 1, is receiving faultless W-one Flit and discovering the defect on (Ri, Ni) link, and in step 2, the FCB is employing idle time to send the result (fault data) to Network Adapter.

VIII. SIMULATION RESULTS AND COMPARISONS

But about the simulation, we are employed the NOXIM (cycle accurate simulator) to implement OSDTM on a Mesh NoC with regarding to Table 7 configuration. The size of Mesh network is considered 5*5 for obtaining more stable results.

Table 7. Pre-setting of simulation

NoC	Flit length(bit)	Packet length(Flit)	link width	Injection rate	Drained packets	Simulation time	Warm-up
5*5	32	12	10	0.01	248	10000	1000

By running simulation, the faults are injected to the NoC up to discovering threshold and even over it. We register the statistics of NoC and so we realized the OSDTM impacts on the NoC parameters which is depicted in in Fig.8.
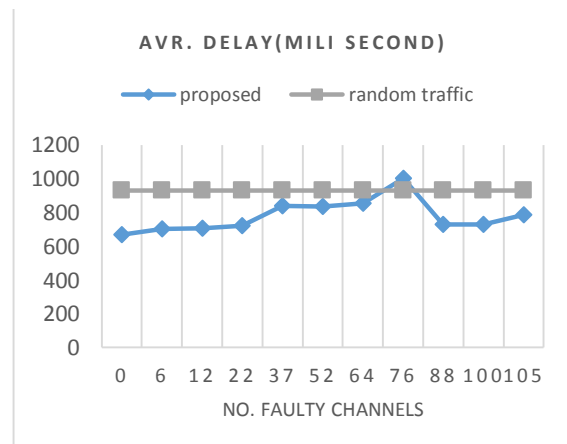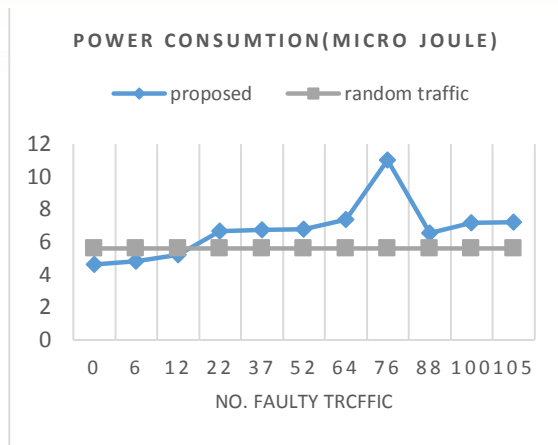
Fig.8. the OSDTM impacts on performance (power consumption and delay)

The sudden climb in the both diagram demonstrates the discovering threshold in the OSDTM. The diagram has reached to final level i.e 75. It is means the OSDTM can discovers 75 faulty links in the one test period. Additional to 75, 25 links is verified in TRC, so, totally 100 faulty links can be discovered through OSDTM in a 5*5 Mesh NoC. The OSDTM has planned to discover the injected faults and specify their positions. The delay and power consumption have increased in discovering threshold point and the decreased, because the FCB has been programed to be enabled but for up to threshold, the FCB is inactive. In the Figure 8, there is another diagram only for comparing the performance of NoC in random traffic and tNV traffic.

IX.   CONCLUSION

In the current paper, an Offline-Structural Distributed Test Mechanism (OSDTM) is presented to discover and emplace short defects in the data links. It is vital, for implementation of OSDTM to establish specific traffic namely to-Neighbors Vector (tNV). In tNV, test packets including head, tail and W-one vectors are passed all the NoC links. The TPP and TRC are located in Network Adapter and TPP produces and sends test Flits to neighbor routers. The OSDTM depend on this fact that the Flits log in the router from various doorways, if are equal it is means there is no fault and if are not equal then in links Flits passed is defects. The simulation statistic are achieved NOXIM demonstrate the OSDTM is 100% test coverage and 82.3% fault discovering and 100% fault emplacement in large scale NoCs. The FCB hardware specification in compare with Vici router hardware is negligible. As a future work, this is will be worth to study on online testing and reusing router resources to design FCB.

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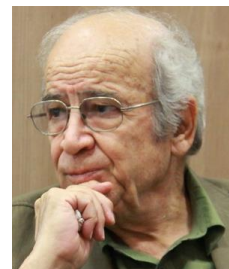
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