

An Improved Active Mixer Architecture for Millimeter Wave Applications

Saeed Zeinolabedinzadeh

Dept. of Electrical & Computer Engineering
University of Tehran
Tehran, Iran
s.zeinolabedinzadeh@ece.ut.ac.ir

Mahmoud Kamarei

Dept. of Electrical & Computer Engineering
University of Tehran
Tehran, Iran
kamarei@ut.ac.ir

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Abstract—Modified active mixer architecture is presented in this paper which improves the gain and noise figure of the mixer considerably. The architecture of the mixer allows wide band operation from very low frequencies up to millimeter – wave regime. Also the proposed architecture makes it possible to use older process options for implementing high frequency mixers with acceptable performance. Simulations using 0.18 μ RF technology files show the efficiency of the mixer. The technology files are based on BSIM 3(V3.2). Accurate transistor and passive component models are obtained by augmenting the technology files with the results of Electromagnetic field solvers.

Keywords- Mixer, CMOS, Millimeter-Wave, gain, Noise Figure, Wide band Response, Electromagnetic field simulation

I. INTRODUCTION

The demand for high speed wireless data communications in one hand and the released wide bandwidth around 60 GHz in some countries on the other hand has motivated the industry to use millimeter – wave frequencies for different applications. Continuous scaling of CMOS technologies made it possible to use this cheap technology for implementing millimeter – wave circuits. The limited maximum operation frequency of CMOS transistors together with the large losses associated with passive elements built on top of lossy silicon substrate degrade the performance of RF circuits considerably. A mixer is one of the important building blocks of every RF front end. Passive mixers have several advantages. They have zero DC power consumption, high linearity and low noise figure. But there are some disadvantages that limit their use in high performance and high dynamic range front ends. The large LO powers are required for driving passive

mixers which impose large power consumption for VCO block. The isolation between different ports of passive mixers is small and their occupied area on the silicon is large. Beside the above disadvantages, the passive mixers impose large losses on the signal. According to basic Friis formula the noise of the succeeding stages would enlarge as large as the loss of the mixer. This is why the sensitivity of the receivers with passive mixer is not adequate while the noise figure of the mixer itself is very small. On the other hand because of the different parasitic paths, limited speed of transistors and lossy substrate, active mixers also do not have acceptable performance at higher frequencies. In this paper we propose a modified active mixer architecture which improves the noise figure and gain of the mixer considerably. Although the analysis are done for the single balanced active mixers, but the concept is general and the idea and equations can be used for the other types of mixer. Through analysis and simulations are used in order to prove the effectiveness of the proposed

Table.1 The list of some of recently reported Millimeter – Wave mixers

Reference	Type	Freq GHz	Gain (dB)	NF	IIP3 (dBm)	Power (mw)	Process
[1]	Double Bal	57 - 65	>2	N/A	-5.6 OP1dbm	24	0.13u
[2]	Double Bal	10 - 35	-3 - 1	N/A	N/A	6	0.13u
[3]	Single Bal	26 - 34	-2.6	13.5 SSB	0.5	20.4	90nm
[4]	Double Bal	22 - 29	1	9	-2	6.9	0.13u
[5]	Double Bal	25 - 75	3±2	N/A	11	93	90nm
[6]	Single Bal	60	8	10	N/A	1.1	0.13u

technique. In order to capture the high frequency model deviation of the Transistor and passive components, extensive 3D field simulations (Sonnet and Momentum) are used and the equivalent lumped element components are modeled. Table.1 shows some of the recently reported mixers implemented for millimeter – wave applications. As indicated from this table the mixers usually consume large amount of power, have small gain and large noise figure. The main cause of this poor performance will be described in the next sections together with the proposed technique which alleviates the problem. Simulation results and conclusions will be presented at later sections.

II. PROPOSED MIXER ARCHITECTURE

Fig.1 shows a typical single balanced active mixer. The operation principal of this mixer is simple. The input RF signal is amplified and converted to current through transistor Mn1. Transistors Mn2 and Mn3 act as switching pair to down convert this current to lower frequency.

As can be seen from this figure, some of the RF current is wasted by the parasitic capacitances present at the common source of switching pairs. This effect lowers the overall gain of the mixer especially by increasing the frequency of input RF signal. The reduced gain on the other hand increases the noise figure of the mixer based on basic Firis formula. This phenomenon is even worse for active DSB¹ mixers.

These stray capacitances shown at Fig.1 have another side effect; they cause switch's noise to find a way to ground through the output node by making a low impedance path to ground at node B in Fig.1.

The other problem associated with this mixer architecture, is the equal current of switches and trans-conductance stage. The trans-conductance stage should conduct enough biasing current, in order to have a sufficient gain, but, on the other hand, the switches should conduct a lower current in order to decrease their noise contribution at the output. The architecture of the SSB mixer shown at Fig.1 does not have enough flexibility to provide optimum biasing for the mixer.

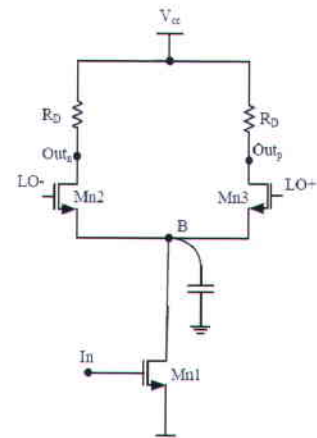


Fig.1 A Typical single balanced Active Mixer

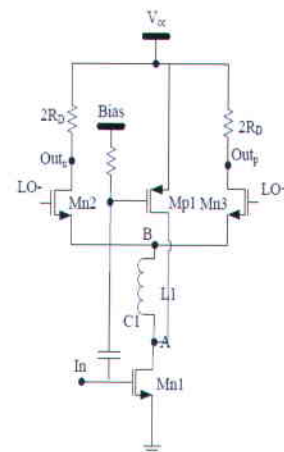


Fig.2 Modified single balanced active mixer

Modified single balanced active mixer architecture is shown in Fig.2. It has similar architecture to the conventional SSB² mixer with some modifications. Inductor L has been added to circuit in order to tune out the parasitic stray capacitances present at nodes A and B. This inductor would prevent the waste of RF signal through these stray capacitances, furthermore by tuning out that capacitances present at node B in Fig.1, the switch's noise would be prevented to flow to the output. In addition, the tuning network at Fig.2 has a very wide band response and does not limit the operation frequency of the mixer core. At lower frequencies, inductor L simply disappears and the circuit is converted to the conventional scheme, but with higher gain which comes from transistor Mp1.

¹ Double Side Band² Single Side Band

tune out smaller capacitances at higher frequencies. From another perspective, the fact that L resonates with smaller capacitance, allows us to increase the size of transistors or increase the inductance value, both of the cases would result in the higher gain for the mixer. Higher inductance would allow the higher RF signal to flow into the switches by making higher impedance at resonance frequency.

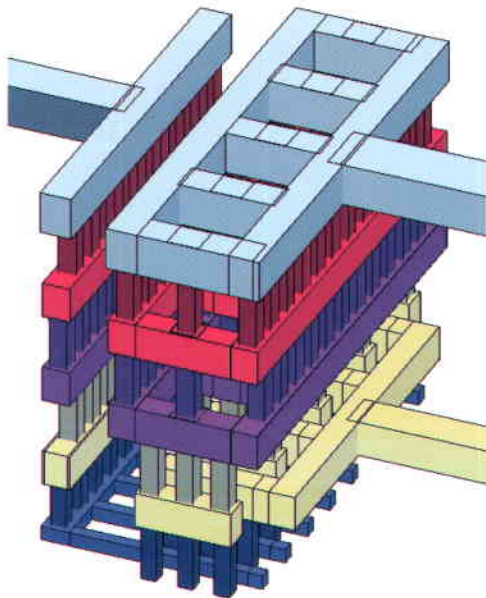


Fig.5 3D view of the internal metalizations of the NMOS transistor

III. DEVICE MODELING STRATEGY

As the operation frequency of RF circuits increases, some parasitic components start to affect the response of the circuit. We need to model the high frequency effects carefully, in order to obtain accurate estimation of circuit behavior. Beside the high frequency accuracy of model, the other important property of the model is its scalability. The models need to be scalable in size in order to be used readily for different designs with different device geometries. There are some high frequency models that have been suggested for the active and passive components, but, just, few of them are accurate and scalable. These models in general use the physical parameters associated with device to make the accurate and scalable model. The transistor models used in this paper are based on the 0.18 μ CMOS BSIM models that we augment them in order to capture the high frequency effects of the device. Passive components have been designed using the accurate 3D electromagnetic field solvers. The next two subsections describe the procedure of the modeling.

A. Transistor Modeling

The main source of discrepancy between the device model and its physical response originates from the internal metallization of the device. These metal lines are not important at lower frequencies but, start to affect the response of circuit by increasing the operation frequency. In order to capture the high frequency distributed effects of these metal lines, we use the 3D electromagnetic field solvers similar to

method used in [9]. Fig. 5 shows the 3 D view of one of NMOS transistors used in the circuit.

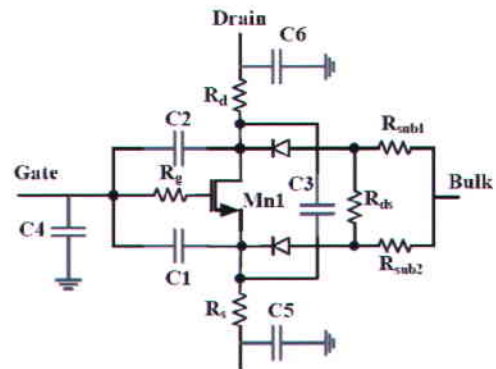


Fig.6 Physical model of the transistor used in this paper

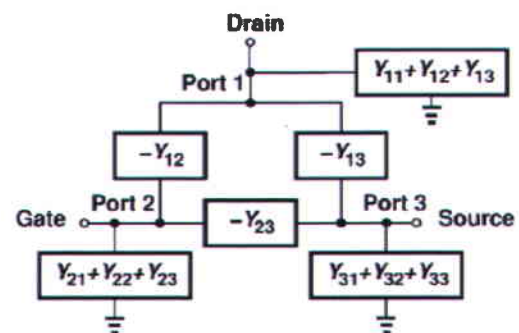


Fig.7 Y parameter representation of the capacitance network of the transistor

The procedure used in this paper, models these high frequency effects from the S parameter data of device structure obtained from 3D field solvers. Looking at Fig.5 again, we excite the structure using 3 ports associated with drain, gate and source of transistor. A substrate stack is constructed containing all metal layers and silicon substrate based on the physical structure of the used technology. The field simulation results would give us the required data in order to augment the transistor model for high frequency operation. Fig.6 shows the physical model of the transistor used in this paper, the internal device Mn1 has been modeled using BSIM models and captures both the small and large signal behavior of the device. Resistors R_g , R_s and R_d model the resistances associated with the junctions of transistor. R_{sub1} and R_{sub2} model the substrate resistance. The diodes model the source and drain junctions of the transistor. All of the parameters shown at Fig.6 are included in the used technology model file except than the capacitors associated with different terminals at the figure. We have added these capacitances to the technology model in order to capture the high frequency effects which originate from the internal metallization of the device as described before. Fig.7 shows the Y parameter representation of the capacitance network of the transistor. Equations 6-11 can be used to find the value of these capacitances.

$$C_1 = \frac{-\text{Im}\{Y_{23}\}}{\omega} \quad (6)$$

$$C_2 = \frac{-\text{Im}\{Y_{12}\}}{\omega} \quad (7)$$

$$C_3 = \frac{-\text{Im}\{Y_{13}\}}{\omega} \quad (8)$$

$$C_4 = \frac{\text{Im}\{Y_{21} + Y_{22} + Y_{23}\}}{\omega} \quad (9)$$

$$C_5 = \frac{\text{Im}\{Y_{31} + Y_{32} + Y_{33}\}}{\omega} \quad (10)$$

$$C_6 = \frac{\text{Im}\{Y_{11} + Y_{12} + Y_{13}\}}{\omega} \quad (11)$$

B. Passive Device's Modeling

Similar to the method used in transistor modeling we have utilized extensive electromagnetic field simulations to model the Inductors and transmission lines used in the circuit. To demonstrate the modeling procedure, the design of an inductor used in this paper is described. The first step in designing the inductor is to find its approximated dimensions. Simple equations used in [10] or the online software [11] can be used to calculate the approximated dimensions of the inductor. Designing large inductors with good quality factor and adequate self resonance frequency is very challenging at millimeter-wave frequencies. The latter is even more difficult to satisfy than the former. As a rule of thumb and as described in [12], higher self resonance frequencies can be achieved if the inductor footprint above the silicon can be made as small as possible; this in turn degrades the quality factor of inductor. There is a trade off between the obtaining higher SRF³ and higher quality factor; one should optimize the dimensions of inductor to get the required results. Fig.8 shows the 3D view of the designed inductor and Fig.9 shows its quality factor calculated from the results of 3D field solver. In order to use this inductor in nonlinear harmonic balance and transient simulations, we need to have a lumped component model for these data.

Different simulators can build the broadband spice model from the generated S parameter data of field solvers. In this paper we use the broadband spice model in our simulations and simplified inductor model for our analytical equations. Fig.10 shows the simplified inductor model used in our calculations. This simple symmetric model contains information about the inductance value, its quality factor and its self resonance frequency. Parasitic capacitances model the SRF of inductor.

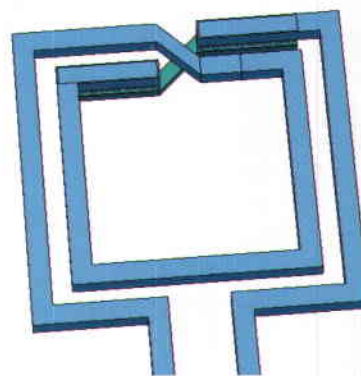


Fig.8 3 D view of the symmetrical Inductor

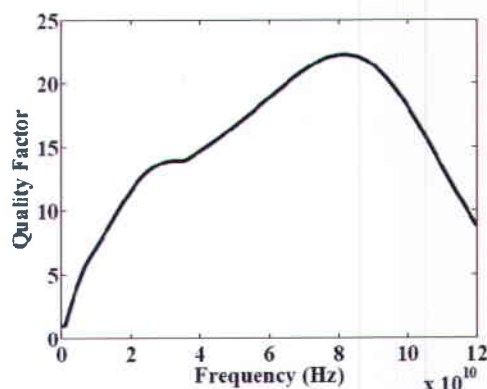


Fig.9 The quality factor of the inductor obtained from electromagnetic field simulations

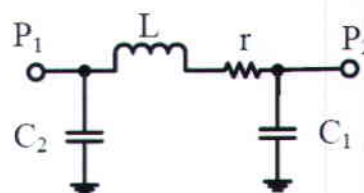


Fig.10 simplified symmetric Inductor Model

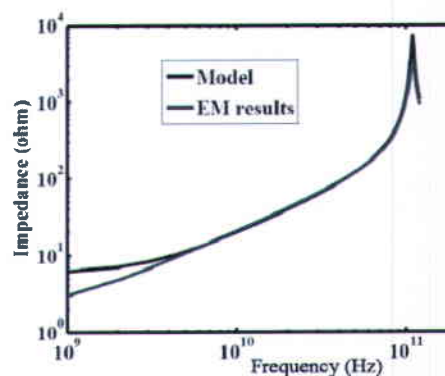


Fig.11 Comparison between the simplified lumped model and the results of EM field solver

³ Self Resonance Frequency

For inductors with high enough SRF, this model matches well with the real inductor behavior. Fig. 11 depicts the comparison between the ac responses of the EM⁴ field solver's results with its approximated π model. As we can see from this figure two plots are matching well especially around the desired frequency which is 60 GHz for this example. This simple model has been created to match the simulated data around the 60 GHz, and that is why we can see slight deviation from the simulation data at very high and very low frequencies. In order to have a broadband matching we need to have more components in the inductor model to model the distributed effects of the inductor at higher frequencies and also more complicated loss mechanism. Fig.9 clearly shows that the quality factor of inductor is not a simple linear function of frequency, as we may ideally expect, however this simple model matches perfectly around the desired frequency and is sufficient for our analytical calculation purposes. Fig.11 also shows almost linear relationship of the impedance of inductor versus frequency in broad range of frequencies which is the expected characteristics of inductors. It is worth to mention at this point that the reported results of several papers as well as the author's experiences in fabrication of the passive components show a close agreement between the result of electromagnetic field solvers and the measured data.

IV. NONLINEAR NOISE CALCULATION

Fig.12 shows the important noise sources of the devices in the mixer, the equivalent noise contribution of every noisy device will be reduced at the input of mixer due to the increased gain of mixer based on basic Firis Formula, furthermore the generated filter at the heart of the proposed mixer, causes a part of the switch's noise to be filtered out. In order to prove the NF improvement of the mixer, a bunch of nonlinear noise simulations were done. Let's first take a look at the noise contribution of the input devices Mn1, Mp1. It is worth to mention here that the flicker noises of the input transistors are up converted to LO frequency and therefore do not have any significant noise component at the IF frequency, as a result, it does not have any significant effect on the overall noise figure of the mixer.

It is clear that white noise sources at the input devices would have the same transfer function as like as the input signal from the input to the output, but addition of the Mp1 amplifying stage would decrease their associated input referred noises. As described before, the Mp1 transistor acts as an LNA here and decrease the input referred noise sources. Assume that v_n^2 and v_p^2 are the equivalent white noise sources of Mn1 and Mp1 at their inputs respectively, the resulted equivalent noise from those sources at the input of the mixer can be calculated using Eq.12.

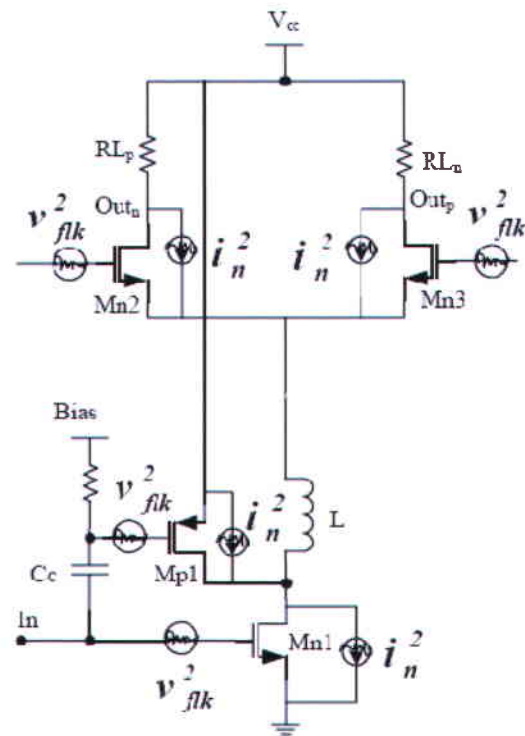


Fig.12 Important noise sources of different transistors in the mixer

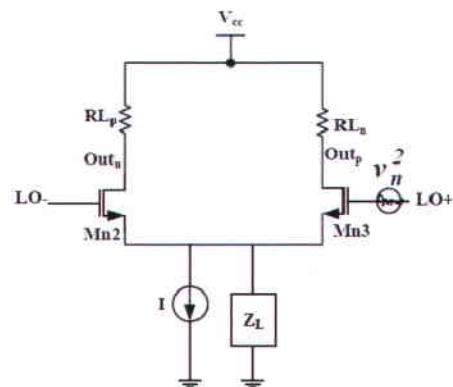


Fig.13 Simplified mixer for noise calculations

As v_p^2 is smaller than v_n^2 and also g_{mp} is smaller than g_{mn} , the equivalent noise at the input of the mixer would be smaller than its previous state before adding Mp1. It means that the overall white noise contribution of the both of Mn1 and Mp1 is smaller than the overall contribution of Mn1 before adding Mp1 and this fact was expected because Mp1 acts as LNA.

$$v_{neff}^2 = \frac{(g_{mn})^2 \cdot v_n^2 + (g_{mp})^2 \cdot v_p^2}{(g_{mn} + g_{mp})^2} \quad (12)$$

In contradiction with the low frequency mixers, the noise contribution of the switches is quite significant at millimeter-wave frequencies. Here we will derive the equations of switch noise at the output of mixer and show how the modified mixer filters out the switch noise. Fig.13 shows the simplified mixer circuit to study the noise behavior of switches.

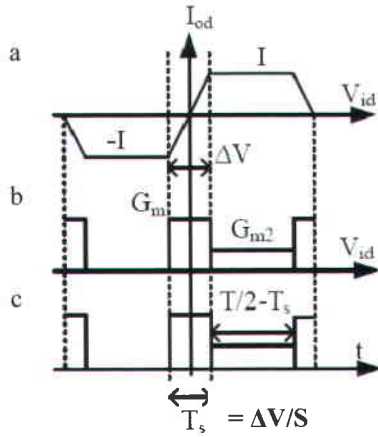


Fig.14 a) Switching Pair I-V curve, b) Transconductance in voltage, c) Transconductance in Time domain

Because of the high impedance of Z_L at lower frequencies, the switch noise can not be injected to the output, except than the switching time instants. During small switching time instant, when both of the switches are conducting, the sources of the switches are virtually grounded and noise has a path to the output. In contrast to the low frequency mixers, Z_L is small at higher frequencies and switch noise can contribute noise to the mixer output at all time instants. Without loss of generality the switch noises are considered just at one side of the differential pair as described in [8]. Switch noise experience a periodic hard switching function called p ($\omega_{LO}t$) showed on Fig.14 while translating to the output.

$$p(\omega_{LO}t) = \sum_n G_m(t - \frac{nT}{2}) + \sum_n G_{m2}(t - nT) \quad (13)$$

$$i_{o,n} = p(\omega_{LO}t) \cdot V_n(t) \quad (14)$$

Where G_m is periodic at twice the LO frequency since there are a couple of zero crossings in each LO period while G_{m2} is periodic at LO frequency. $V_n(t)$ is the switch noise referred to switch input which is white and stationary. Eq.14 is the differential current noise at the output which is white and cyclostationary and can be expressed as the product of p ($\omega_{LO}t$), a periodic and deterministic function, and V_n the white and stationary switch input-referred noise. The auto correlation of white noise is calculated as

$$Ri_{o,n}(t+\tau, t) = p(t) \cdot p(t+\tau) \cdot R_{V_n}(\tau) \quad (15)$$

The power spectral density is calculated by averaging $Ri_{o,n}$ over one period and transforming the result, now only a function of τ , into frequency domain. The power spectral density of the output current noise is

$$i_{o,n}^2 = \frac{1}{T} \int_{-T/2}^{T/2} p^2(t) dt \cdot V_n^2 \quad (16)$$

$$V_{nout}^2 = \left\{ \frac{2}{T} (G_m^2 T_s \cdot 2R_L^2) + \frac{1}{T} (G_{m2}^2 \cdot (\frac{T}{2} - T_s) \cdot R_L^2) \right\} V_n^2$$

$$k(w) = \frac{G_{m2}}{G_m} = \frac{1}{0.5 + G_m \cdot Z_L(w)}, V_n^2 = \frac{4KT\gamma}{G_m} \quad (17)$$

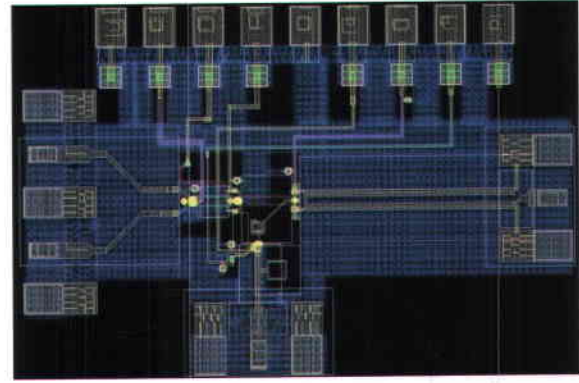


Fig.15 Layout of the 60 GHz Mixer

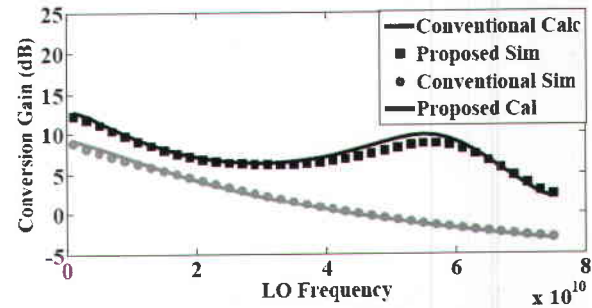


Fig. 16 Gain improvement of the modified mixer architecture

$$T_s = \frac{\Delta V}{S}, G_m = \frac{2I}{\Delta V} \quad (18)$$

$$S = 2A \cdot \omega_{LO} \quad (19)$$

$$V_{nout}^2 = 4KT\gamma R_L^2 \cdot \left(\left(1 - \frac{k^2(w)}{4}\right) \times \frac{2I}{\pi A} + 0.5 \cdot G_m \times k^2(w) \right)$$

V_{nout}^2 at the above equations is the differential output noise at the output of mixer and S is the slope of input differential LO signal. Eq.20-22 shows the frequency response of the Z_L , as we can see from this equations, there is resonance frequency at ω_r in which Z_L has a local maximum. At this frequency switch noise contribution at the output noise will be reduced or in other words, the switch noise will be filtered out at this frequency.

$$Z_L = \frac{G(w)}{H(w)} \quad (20)$$

$$H(w) = j\omega \cdot (C_1 + C_2 - LC_1C_2 \cdot \omega^2) - rC_1C_2 \cdot \omega^2 \quad (21)$$

$$G(w) = (1 - LC_2\omega^2) + jrC_2\omega$$

$$\omega_r = \frac{1}{\sqrt{LC_1C_2 / (C_1 + C_2)}} \quad (22)$$

The equations derived for the gain and noise are perfectly matched with the simulations.

V. SIMULATION RESULTS

To show the effectiveness of the modified architecture, a mixer was designed to operate in the wide frequency range from DC up to 60 GHz. Layout of the mixer is shown in Fig.15. This design includes



an on chip Marchand Balun, an input matching network and a couple of buffer stages.

The selected RF and IF frequencies for this mixer, are 60GHz and 100 MHz respectively. The derived equations in the previous sections for the gain and noise response of the millimeter-wave mixer, would be compared with the result of Harmonic balance simulations in this section. The simulated gain comparison of the modified mixer and the conventional one is shown at Fig.16. This figure also demonstrates the result of our gain calculations for both of the modified and conventional mixers. As can be seen from this figure, the calculations perfectly match the simulated data. There is slight deviation between the calculated gain and simulated one around the 60 GHz. As we stated before, the nonlinear hard switching operation was estimated with multiplication by square wave, but this assumption is not perfect around the resonance frequency of the filter embedded in the body of the mixer. Transient simulation results show that, at this frequency the hard switching action, can be perfectly estimated by multiplication of a sinusoidal signal rather than square wave one. This result is predictable, since the higher harmonics of switching currents are filtered out with the filter in the body of the mixer. As can be seen from the Fig.16, the modified mixer has near 10dB improvement of gain around the 60 GHz. The lower frequency gain improvement indicates the gain improvement as result of class AB complementary input stage.

Fig.17 depicts the output rms white noise voltage contributed by the switches for both of the conventional and modified structure. This figure also depicts the result of our nonlinear noise calculations in comparison with the simulated data. As can be seen from this figure, the nonlinear calculations match perfectly with the result of simulations. It is worth to mention that to the authors' best knowledge, these kinds of noise calculations have never been done for the millimeter-wave frequencies. As we can see from this figure; the white noise associated with the switch is filtered out as predicted before. The method used for the noise calculation is general and similar equations can be derived for the other noise sources at the mixer. It is worth to note that these noise filtering mechanisms together with the gain improvement of the mixer, translates to the significant NF improvement. Fig.18 shows the noise figure of the modified mixer in comparison with the conventional SSB mixer. As can be seen from this figure, there is - more than 8 dB noise figure improvement for the proposed mixer. The over all noise figure of the modified mixer is almost 13 dB for the operation around 60GHz, it is worth to mention that these results are obtained while working around the transition frequency of the used technology. It is clear that, better performances could be obtained from the faster technologies. Finally it is worth to investigate the linearity behavior of the modified mixer. Looking again at Fig.2, we expect some linearity degradation due to the nonlinearities of the added PMOS

transistor, Mp1. We used two tone test for measuring the IP3 of the mixers. The measured IP3's are shown on table.2 and indicates 3.9 dBm IP3 degradation.

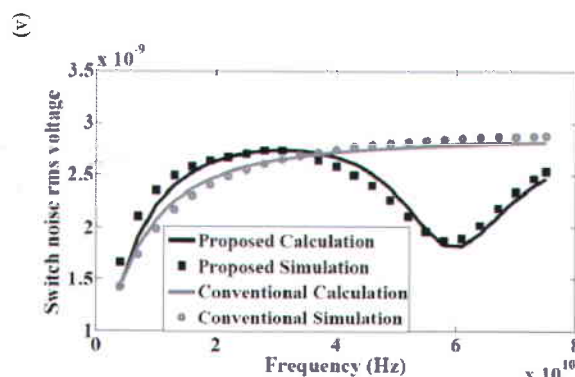


Fig. 17 output rms noise voltage resulted from switch

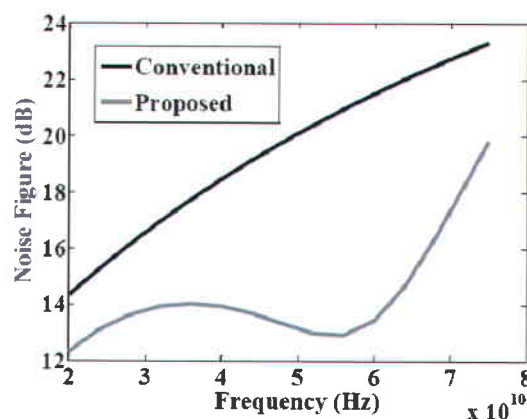


Fig.18 Noise Figure Improvement of the mixer

Table.2 Simulated IP3 of the mixers

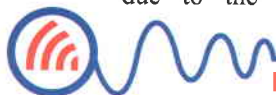
Mixer Type	Conventional SSB	Modified
IP3 (dBm)	3.5	-0.37

VI. CONCLUSION

Modified active mixer architecture is introduced and extensively analyzed in this paper. It achieves 10 dB of gain and 8dB of noise figure improvement over its conventional active SSB counterpart at frequencies as much as the f_T of the used technology. The proposed mixer core has wide band operation from very low frequencies up to higher frequencies as much as the f_T of the used technology. Accurate transistor and passive models are obtained by augmenting the technology files with the results of Electromagnetic field solvers. Simulations were done using 0.18u RF technology files to verify the effectiveness of the method.

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Saeed Zeinolabedinzadeh obtained his B.Sc. degree in electrical engineering from Iran University of science & Technology, and the M.Sc. degree in Electrical Engineering from Sharif University of Technology. During his Master, he worked on Sigma-Delta modulators for communication applications. He worked on his PhD at University of Tehran. Saeed was the recipient of the 2010 IEEE-CAS pre-doctoral scholarship. His research interests include designing RF and Millimeter-wave circuits for communication applications.



Mahmoud Kamarei received his M.Sc. degree in Electrical Engineering from the University of Tehran in 1979, CES in Telecommunications from the Ecole National Supérieure des Telecommunications of Paris in 1981, his Diplôme d' Etudes Approfondies and his Ph.D. degree from Institute National Polytechnique de Grenoble (INPG) - France, both in Electronics, in 1982 and in 1985. Since 1982, he has been a researcher at INPG's Laboratoire de l' Electromagnetisme, Micro-Ondes et Optoelectronique. Mahmoud Kamarei also was Maitre de Conférences at J. Fourier University of Grenoble until September 1991. He worked as Director of Electrical & Computer Engineering Department (1994–2002), Professor and Associate Dean in Research of the Faculty of Engineering (2002– 2006) and Vice-president for Academic Affairs at the University of Tehran (2006-2009). Mahmoud Kamarei has been the Dean of University College of Engineering - University of Tehran since August 2009.

