

Research Note

Sensitivity Analysis of Shielded Coupled Interconnects for RFIC Applications

Mohammad Moghaddam Tabrizi

Advanced VLSI Lab., Department of Electronics,
School of ECE, University College of Eng.,
University of Tehran, Tehran, Iran
Moghaddam@gmail.com

Nasser Masoumi

Advanced VLSI Lab., Department of Electronics,
School of ECE, University College of Eng.,
University of Tehran, Tehran, Iran
nmasoumi@ut.ac.ir

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Abstract— In this paper the sensitivity of on-chip interconnects to Si CMOS process parameters in two different test structures are reported; two coupled lines with shielding, and without shielding. Simulations are performed using HSpiceRF to emulate the state-of-the-art and the future technologies for the test structures. Some important parameters characterizing the coupled interconnects have been examined. Shielding effectiveness on crosstalk reduction is computed using HSpiceRF simulation results in order to compare the efficiency of shielding structures with different process parameters. Additionally we investigate the influence of the process parameters in deep sub-micron technologies on the transmission, reflection, near-end, and far-end crosstalk characteristics of the coupled interconnect with and without the presence of shielding lines.

Keywords-Interconnects, Shielding, Sensitivity Analysis.

I. INTRODUCTION

In the recent years, wireless devices such as pagers, cellular and cordless phones, global positioning system devices (GPS) and personal communication systems have been penetrated in all aspects of our daily lives. Several mobile and wireless communication standards have been widely used covering the frequency range from 900 MHz to 5.9 GHz, e.g. global system for mobile (GSM), code division multiple access (CDMA), Bluetooth, IEEE802.11, and so on. As being seen from the market point of view, the cost and ease of system implementation are two imperative factors [1], [2]. Thereby, there is an increase of interest in the development of radio-frequency system-on-chip (RF-SoC) that integrates RF, analog, and digital circuits altogether on a single chip. Besides the circuit design,

the choice of the implementation technology is also very important and complicated. Compared with other available technologies, such as bipolar CMOS (BiCMOS), GaAs metal-semiconductor field-effect transistor (MESFET), heterojunction bipolar transistor (HBT), CMOS technology is considered as the most attractive and promising one in the future [3].

Because of the combination of the increasing circuit complexity and higher operating frequencies of CMOS ICs, the circuit performance becomes more and more dependent on to the interconnects. On the other hand, the growing speed of the CMOS process technology is truly spectacular. However, the process parameters are optimized to improve the circuit performance, the effects of the process parameter variations on the interconnects have rarely been reported in the literature. In the previous works [4], [5] effects of the process parameters, such as conductivity

of the substrate, the thickness, and the permittivity of the dielectric, as well as the conductivity of the metallic conductor on the transmission and reflection characteristics of a single and coupled interconnects, have been examined. Because of large density of interconnects in real cases, the crosstalk among interconnects is one of the most important internal EMC problems. Hence, it would be very useful to explore information about the sensitivity of interconnects to parameters that affect the crosstalk. In [5] the dependence of the transmission, reflection, far-end, and near-end crosstalk of two coupled interconnects on the process parameters has been addressed. In this paper, the crosstalk among the on-chip interconnects is analyzed, and the influences of the process parameters in deep sub-micron technologies are investigated in presence of shielding line. Also, the trend of shielding efficiency variations in new technologies is demonstrated. In this paper, the top metal layer interconnects are considered, because it is the most commonly allocated for routing critical high-frequency paths. This paper is organized as following. In Section 2, a test structure for the crosstalk and the shielding efficiency simulation is presented. The influences of the process parameters on the coupled interconnect is examined in Section 3. Shielding efficiency is demonstrated in Section 4. Finally, the paper is concluded in Section 5.

II. TEST STRUCTURES

In order to analyze the crosstalk sensitivity of two coupled interconnects, a large number of interconnect structures along with various process parameters are needed. Two possible choices may be considered. The first one is to design and fabricate all the possible test structures with different process parameters, which is extremely costly, time-consuming, and most probably impractical. An alternative approach is to use interconnect simulation capability of HSpiceRF in various structures. The cross view of two test structures are shown in Fig. 1. Two test structures with several sets of process parameters are designed and simulated using a 0.18 μm RF CMOS process. They are thoroughly investigated in the following sections where the values for geometrical dimensions of test structure are summarized in Table. 1. As shown in Fig. 1, two different structures are employed; Structure 1: two coupled lines; Structure 2: two coupled lines with the same spacing in the presence of a shielding line. The interconnect 1 is assumed to be the active line, and the interconnect 2 is assumed to be the victim line. Also, an input signal is applied to the port 1. Eventually, the S-parameters S11, S21, S31, and S41

Table 1. The values for geometrical dimension of test structure

Parameter	Length (L)	Width (W)	Height (h)	Line spacing (S)
Value	400 μm	5 μm	3.5 μm	10 μm

(all in dB) are extracted using HSpiceRF.

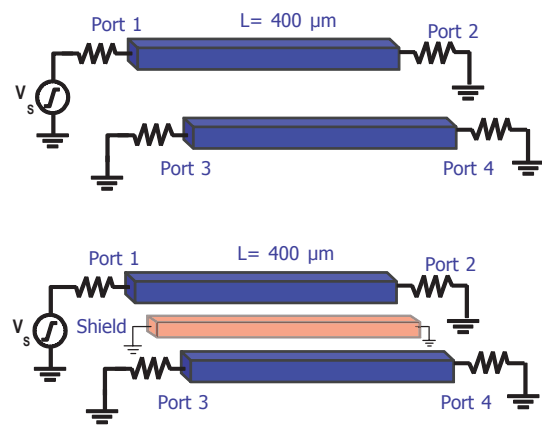


Figure 1(a). The test structures; Shielded and unshielded structures

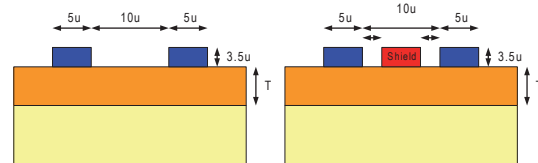


Figure 1(b). The cross section of test structures and dimensions

III. INFLUENCE OF THE PROCESS PARAMETERS

Four major process parameters are considered, namely conductivity of the substrate, permittivity of the dielectric, thickness of the dielectric, and conductivity of the metallic conductor. During the simulations, these four parameters are changed in an order. Only one parameter is changed each time, while the rest are kept constant. The variation range of each parameter is chosen to emulate the state-of-the-art and the future Si CMOS technologies.

A. Conductivity of the Substrate

In the CMOS technology, the performance of the on-chip interconnects is significantly affected by the lossy nature of the silicon substrate [6]. In recent technologies, the substrate conductivity (σ) is approximately assumed to be 6–50 S/m (2–18 Ω-cm) [7]. In order to study the influences of the substrate conductivity, typical values of 6 S/m, 50 S/m, and 5×10^3 S/m, are used in the simulations of two test structures. Comparisons of S11, S21, S31, and S41 for various values of the substrate conductivity are shown in Fig. 2. Also, Fig. 3 illustrates the scattering parameters of two coupled lines in the presence of the shielding line to study the effects of the process parameters on the shielding properties. The different values of the substrate resistance results in deviation of S11 by 10%, but in the second structure, the presence of shielding line provides parallel capacitance which degrades the amount of S11 from -12.5 dB to -15.5 dB at 15 GHz. Consequently, in this circumstance the deviation of S11 is shrunk to 4%.

As a matter of fact, the amount of power leakages through the parasitic capacitances increases at high frequencies, thus S21 decreases. The presence of the shielding line provides more parasitic capacitances and therefore, the amount of power leakage increases through the entire line. Consequently, it is evident that the shielding line degrades S21 by 10% at 10 GHz, and also the deviation of S21 decreases from 8% in structure 1 to 3% in structure 2 at 15GHz when the



different values of substrate resistances have been considered. Generally, the bulk resistance introduces complex effects on S21 and it doesn't follow a certain trend [4].

In both structures, it can be observed that coupled interconnects with large S21 suffers more from the far-end crosstalk, while near-end crosstalk is considerable in the coupled interconnects with large S11, because the victim line energy is originated from the active line. Also, the smaller substrate resistance, the inferior near-end crosstalk. As shown in Fig. 3, the shielded structure lowers the amount of the near-end crosstalk about 7 dB in substrate conductivity of 6 S/m and 50 S/m, and about 9 dB in the structure with substrate conductivity of 5000 S/m. Therefore, there is a little bit high shielding effectiveness in the low substrate resistance, because of the presence of well-grounded shielding line with respect to the low resistance substrate. The amount of the far-end crosstalk in the second structure doesn't vary with different substrate conductivities, so shielding effectiveness for far-end crosstalk is independent of the substrate resistance.

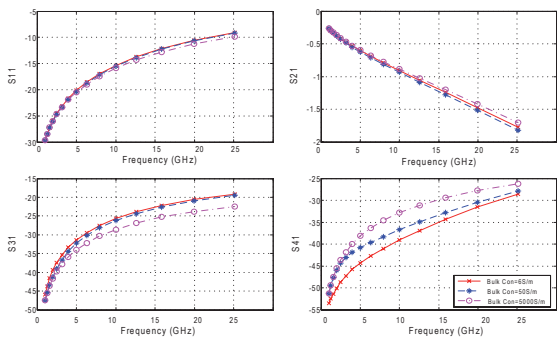


Figure 2. Comparison of S-Parameters with substrate conductivity variation in the two simple coupled lines

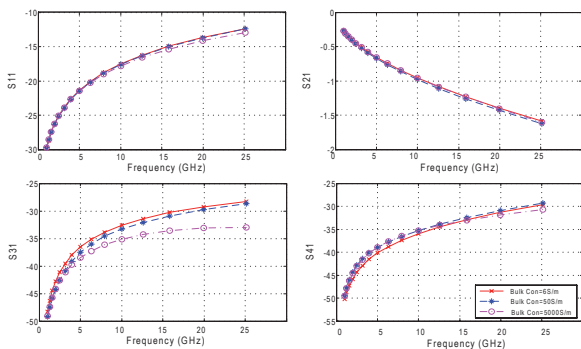


Figure 3. Comparison of S-Parameters with substrate conductivity variation in the two Shielded coupled lines

B. Conductivity of the Metallic Conductor

Due to its higher conductivity ($\sim 5.8 \times 10^7$ S/m), copper metallization has been introduced for the aggressive interconnects instead of traditional Al ($\sim 2.7 \times 10^7$ S/m) or AlCu ($\sim 3.3 \times 10^7$ S/m) metallization [8]. As shown in Fig. 4, S11 is inversely proportional to the conductivity of interconnects at low frequencies. It means that higher conductive lines, smaller reflections. While, the influence of conductivity on S11 becomes negligible when the frequency approaches several gigahertz, because the impedance is dominated by the inductance and capacitance instead of the resistance at high frequencies. As illustrated in Fig. 5, adding the

shielding line in structure 2 degrades S11 from -11 dB to -12 dB in the low conductive lines. Also, the amount of degradation in the high conductive lines is from -13 dB to -15 dB at frequency of 15 GHz.

The S21 of both structures in Fig. 4 and Fig. 5 follows the same trend which is discussed in the previous section. In the structure 1 the forward transmission capability (S21) is downgraded from -1.2 dB in the high conductive lines to -2.2 dB in low conductive line at frequency of 15 GHz. The Shielding line in the structure 2 has a little effect on S21 and caused a little bit of degradation about 0.1 dB at frequency of 15 GHz.

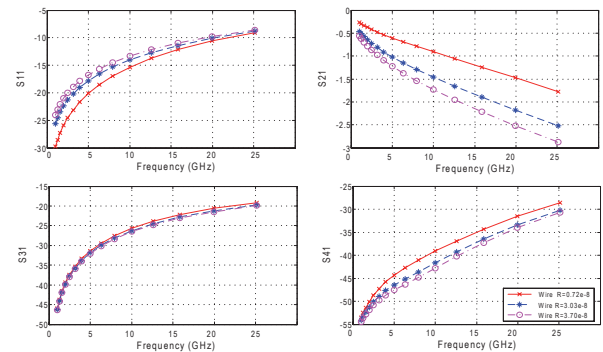


Figure 4. Comparison of S-Parameters with wire resistance variation in the two simple coupled lines

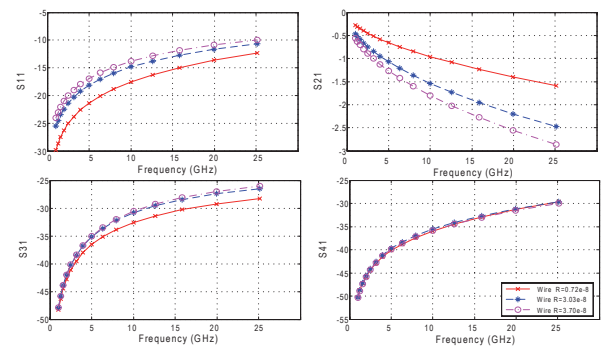


Figure 5. Comparison of S-Parameters with wire resistance variation in the two shielded coupled lines

As shown in Fig. 4, the near-end crosstalk is not strongly affected by the variations of the line conductivity which is quite normal and predictable. Fig. 5 shows that the presence of shielding line degrades near-end crosstalk about 5 dB for the low conductive line and 8 dB for the high conductive line at frequency of 10 GHz. Therefore, it is clear that shielding efficiency becomes maximum for the low resistance line. In both structures it can be observed that the coupled interconnect with large S21 suffers more from the far-end crosstalk. On the other hand, Fig. 5 shows that the far-end crosstalk has a small deviation in different conductivity of lines. However, there is a large amount of transferred power because of large S21 in high conductive lines; resulted large far-end crosstalk is canceled with the large shielding effectiveness.



C. Distance from the Substrate

Due to the increase in the number of the metal layers, the vertical dimensions do not scale down in contrast to the horizontal dimensions. Advanced CMOS technologies utilize up to 10 metal layers. Top metal layer can be far from the Si substrate about 16 μm [9]. In our experiment, the three chosen distances of the line from the substrate are 5.5 μm , 10 μm , and 16 μm . As shown in Fig. 6, a further distance from the substrate means a smaller capacitance and consequently, results in higher S11. The presence of shielding line increases the parasitic capacitance and thus, degrades S11 about 4 dB in the large distances and 3 dB in the small distances at frequency of 15 GHz. Also, the effect of different distance from the substrate on the S11 is about 20% in the structure 2 and about 30% in the structure 1.

The amount of power leakages increases through the parasitic capacitance at high frequencies and subsequently, S21 decreases. Based on our discussions in previous sections, the amount of S21 is inversely proportional to the S41 which is illustrated in Fig. 6 and Fig. 7. The interconnect line with a long distance from the substrate is more affected by the shielding line. It is illustrated that the S21 of line with T=5.5 μm is affected by shielding line about 0.05 dB, and when the line distance from substrate reaches to value of T=16 μm , the amount of shielding line effects on S21 is become to about 0.25 dB.

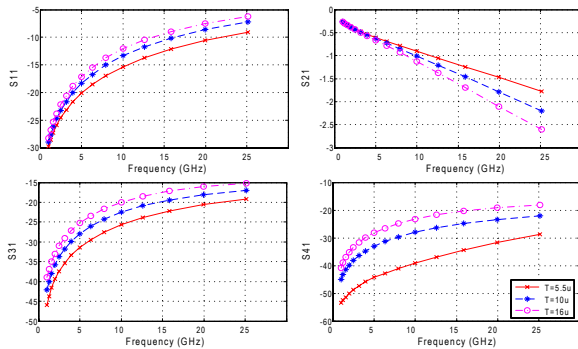


Figure 6. Comparison of S-Parameters with oxide thickness variation in the two simple coupled lines

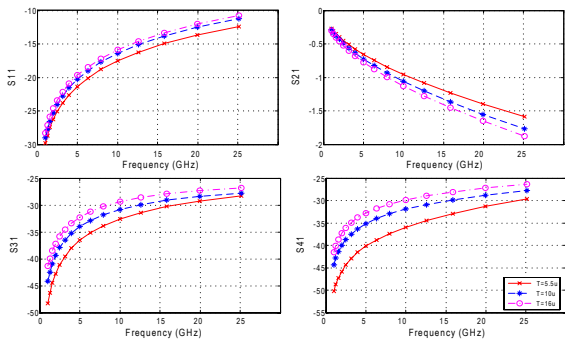


Figure 7. Comparison of S-Parameters with oxide thickness variation in the two shielded coupled lines

On the other hand, Fig. 6 demonstrates that the amount of crosstalk increases on the line which is at long distance from the substrate. As illustrated in Fig. 7, shielding line degrades the near-end crosstalk about 8 dB and 11 dB for T=5.5 μm and T=16 μm at the

frequency of 15 GHz, respectively. So it can be demonstrated that the shielding efficiency has its maximum values at the higher distance from the substrate. Far-end crosstalk is degraded by shielding line about 2 dB and 8 dB for T=5.5 μm and T=16 μm at the frequency of 15 GHz, respectively. Also, it is affected by S21 and generates different shielding efficiencies for near-end and far-end crosstalk.

D. Permittivity of the Dielectric

Recently, numerous low-k materials across a wide range of dielectric constants, from air ($k = 1$) to fluorinated oxides ($k = 3.6$), have been used for interconnect systems [8]. The values of 4.0, 3.6, and 1 are used as the relative permittivity (k) of the dielectric for the simulation. The values correspond to the traditionally used silicon dioxide and novel low-k materials. Corresponding comparisons of S11–S41 are given in Fig. 8 and Fig. 9. As shown in Figures, S11 and S21 are inversely proportional to the relative permittivity of the dielectric. It follows the same trend as discussed for the other parameters. As shown in Fig. 9, the presence of shielding line slightly degrades S11 about 2 dB and 3 dB for $\epsilon=4$ and $\epsilon=1$, respectively.

The amounts of S21 in both structures are independent of the dielectric constant; also the presence of the shielding line has no effect on S21, too. From Fig. 8, it can be observed that the interconnect structures using high dielectric permittivity materials suffer from crosstalk effects. The structure with large dielectric permittivity materials has great coupling capacitances, so the same energy in the active line produces greater crosstalk effects. Consequently, the near-end crosstalk is proportional to k . As shown in Fig. 9 employing shielding line degrades the near-end crosstalk about 8 dB and 9 dB for $k=4$ and $k=1$ at the frequency of 15 GHz respectively. So different values of k have a negligible effect on shielding efficiency.

IV. SHIELDING EFFECTIVENESS

Shielding effectiveness (SE) is the parameter that shows the efficiency of the shielding structures in the blocking of the crosstalk noise. It is given in dB and defined in (1).

$$SE_{(Near-End)} = \frac{S_{31(shielded)}}{S_{31(unshielded)}} \tag{1}$$

$$SE_{(Far-End)} = \frac{S_{41(shielded)}}{S_{41(unshielded)}}$$

Influence of different process parameters on the shielding effectiveness based on crosstalk simulations is illustrated in Fig. 10. As shown in this plot, the shielding efficiency increases in the interconnect lines far from substrate, and with high conductivity substrate. Also, shielding efficiency degrades with conductor resistance increases, and dielectric constant has a negligible effect on the shielding efficiency.



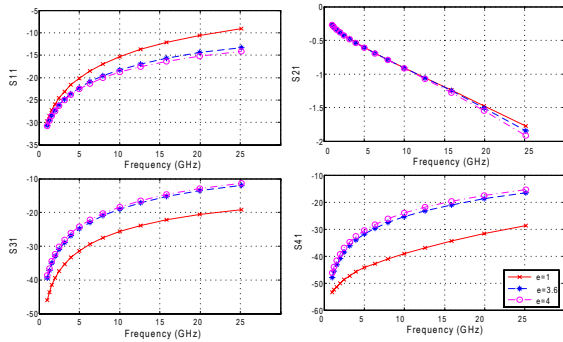


Figure 8. Comparison of S-Parameters with permittivity variation in the two simple coupled lines

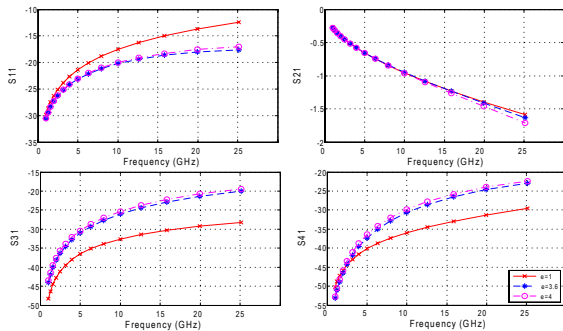


Figure 9. Comparison of S-Parameters with permittivity variation in the two shielded coupled lines

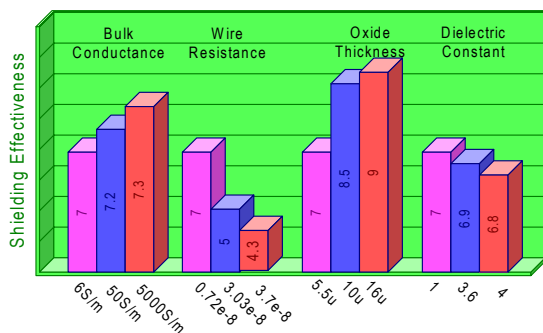


Figure 10. Comparison of shielding efficiency with process variation

V. CONCLUSION

The sensitivity of the on-wafer coupling interconnects in the shielded structure of the current and future Si CMOS technology has been investigated based on the simulation of the 0.18- μ m RF CMOS process. By comparing the sensitivity of the shielded and unshielded two coupled interconnects, it is observed that the reflection (S11) and transmission (S21) of the coupled interconnects with shielded structures follow the same trend when the process parameters (conductivity of the substrate, permittivity of the dielectric, thickness of the dielectric, and conductivity of the metallic conductor) take different values. Both the far-end crosstalk (S41) and the near-end crosstalk (S31) are proportional to the conductivity of the conductors and the distance between the conductors and the substrate. It is highlighted that increasing the distance between the interconnect lines and the substrate can improve the shielding efficiency. Hence, shielding line is more desirable at the top level of metal layers. On the other words, there is no need for the interconnect lines near

the substrate to have shielding line. As for the dielectric permittivity, S41 and S31 are inversely proportional to it. The impact of the substrate conductivity is more complicated, no monotonic relationship can be observed.

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Mohammad Moghaddam Tabrizi received his B.Sc. from Iran University of Science and Technology (IUST) and his M.Sc. degrees from University of Tehran, Tehran, Iran, in 2002 and 2005, respectively, both in electrical and computer engineering. He is currently a Ph.D. candidate in University of Tehran. The main topic

of his research has focused on Analog RFIC Design. His research thesis topic is Linear and High Efficiency Power Amplifier for WiMAX Application.



Nasser Masoumi (S'90–M'96) received the B.Sc. and M.Sc. degrees from University of Tehran, Tehran, Iran, in 1988 and 1990, respectively, both in electrical and computer engineering, and the Ph.D. degree in electrical and computer engineering from University of Waterloo, Waterloo, ON, Canada, in 2001.

Dr. Masoumi joined the school of Electrical and Computer Engineering, University of Tehran, in 1991. He is currently an Associate Professor, the head of Department of Electronics, and founder of Advanced VLSI and RFIC

Laboratories, in the University of Tehran. He has also been director of Science and Technology Park of University of Tehran from 2005 to 2006.

The main topics of his research has focused on: interconnects, nano-wires, carbon nanotubes (CNTs), VDMS and nano VLSI circuits and systems design, CAD for VLSI, power management in VLIS, on-chip crosstalk, signal integrity and reliability issues.

His research interests also include substrate coupling, modeling and synthesis of RF/microwave spiral inductors, RF wireless communications transceiver and power amplifier design, mixed-signal IC design, CMOS high performance and low-power analog and digital design.

Dr. Masoumi has been the head of Department of Electronics in School of ECE, College of Eng., University of Tehran since 2009. He is a member of several internationally recognized scientific and industrial organizations and journals. He has also served as a scientific committee member for many conferences and symposiums.

